REMARKS

Claims 1-29, 31 and 32 are pending in the present application. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

The Examiner is thanked for the withdrawal of the finality of the previous office action.

Turning now to the rejections, Claims 1, 2, 8, 28, and 32 were rejected under 35 U.S.C. §102(b) as being anticipated by Martel et al. (U.S. Patent No. 5,887,165). Claims 1, 2, 7, 11, 19, 29, and 31 were also rejected under 35 U.S.C. § 102(b) as being anticipated by O'Brien (U.S. Patent No. 6,107,876). The other dependent claims were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien, in view of one or more of a number of references. These rejections are respectfully traversed for the following reasons.

The Application claims have, from the outset, been directed to a pre-amplifier apparatus and are now limited to apparatus including "reconfigurable circuit means which are configured in real time under control of configuration data". In particular, claim 1 recites software definable pre-amplifier apparatus including one or a plurality of

reconfigurable circuit means which are configured in real time under control of configuration data allowing the reconfigurable circuit means to implement in hardware different signal processing functions required for at least one of different digital signal processing algorithms and different audio processing protocols, a local memory coupled to the reconfigurable circuit means. The local memory stores the configuration data and is operative to supply configuration data to the reconfigurable circuit means when a different signal processing function is to be performed. The apparatus further includes a host processor and associated program memory means for updating configuration data in the local memory and controlling and monitoring operation of the apparatus. This is not taught, disclosed or made obvious over the prior art.

In Applicant's previous response, Applicant provided arguments to why the reconfigurable logic according to the present invention is different than that implemented in an FPGA. These arguments were accompanied by examples of Xilinx FPGAs showing that it is not possible to reconfigure an FPGA in real time to implement the functions described in the present application. These arguments are incorporated herein by reference. Further arguments will be presented below.

Claim 1 recites a software definable pre-amplifier apparatus including one or a plurality of reconfigurable circuit means which are configured in real time under control of configuration data allowing the reconfigurable circuit means to implement, in hardware, different signal processing functions required for at least one of different digital signal processing algorithms and different audio processing protocols, and a local memory coupled to the reconfigurable circuit means. The local memory stores the configuration data and is operative to supply configuration data to the reconfigurable circuit means when a different signal processing function is to be performed. A host processor and associated program memory means are also included in the apparatus for updating configuration data in the local memory and controlling and monitoring operation of the apparatus. This is not taught, disclosed or made obvious by the prior art of record.

Martel (U.S. Patent No. 5,887,165) mentions the use of a System Programmable Gate Array (SPGA). However, a SPGA is a device, which contains some fixed ASIC circuitry and FPGA circuitry. The idea was taught by Martel is to provide a device that had the advantages of both types of device. The fixed ASIC circuitry was generally used to implement processor cores and peripheral interface function and memory. The

reason for doing this is that to implement functions, such as processor cores, etc., in a pure FPGA device would mean that these it would take up most of the FPGA circuitry and leave little, if any, of the FPGA circuitry to implement other functions. As this would also be a large device, it would not be economically viable to do this, because FPGAs are very expensive. Therefore, these fixed cores would be implemented on a device surrounded by some FPGA circuitry. In fact, many of these devices never made it to market, as they resulted in conflicting, if not confusing, product stand points.

Consequently, as the reconfigurable circuitry on a SPGA is FPGA based, the same arguments Applicant's provided in the previous response regarding FPGAs still apply. That is, it is not possible to reconfigure either an FPGA or SPGA in time to dynamically reconfigure the logic circuits to implement different processing functions as described in Applicant's application.

Further more, Martel et. al. states that the state of the field programmable gate array remains constant as long as power is applied to the gate array's circuitry (column 4, line 51). Consequently, in Martel's system, there is no need to implement real time dynamically reconfigurable logic as described and claimed in Applicant's application and claims. In fact, the real time reconfiguration described by Martel et.

al. relates to updating new application functions in relation to new standards, etc., to ensure they are backward compatible with legacy systems and that is cheaper and more convenient to implement than system upgrades. This is the usual use of FPGAs, hence they are field programmable.

To those familiar with the art, it is understood that "real time" means performing a function in such a time that it does not halt or disrupt the normal flow, i.e., not having to stop or slow down a system. Consequently, there are different timing granularities with regards to reconfiguring in real time. Applicant's dynamically reconfigurable logic is reconfigurable in microseconds, allowing the reconfigurable logic circuits to implement different processing functions in hardware in real time. This cannot be achieved with FPGAs due to their relative long reconfiguration times.

For these reasons, Applicant respectfully submits that claim 1 is patentable over Martel et al.

In response to paragraph 4 of the office action, the Examiner outlines the fact that Applicant implements the technology in an ASIC and an ASIC is mentioned by O'Brien (U.S. Patent No. 6,107, 876). What is actually described (column 3, line 58) is, "All or part of [the] amplifier is implemented in ASIC and/or FPGA". There is no mention anywhere in the patent that the circuitry is reconfigurable or

real time reconfigurable as described and claimed in the present application. O'Brien just teaches normal fixed circuitry. In fact, if all the amplifier circuitry can be implemented in an FPGA, as stated by O'Brien, then the circuitry cannot be dynamically reconfigurable for the reason Applicant has provided previously regarding FPGAs. The sentence (column 3, line 58), "All or part of amplifier is implemented in ASIC and/or FPGA", means that if an ASIC is used, an FPGA must also be used in conjunction with the ASIC. The reason for this is that the flexible design options are implemented in the FPGA, not in the ASIC. No reconfigurable circuit or flexible design option are implemented in the ASIC. Therefore, it follows that an ASIC implementation of the amplifier circuitry is fixed circuitry that does not implement any real time reconfiguration. In addition, all of the digital sections of the amplifier are described as separate units that are concatenated together in a single device. None of the logic in the device is reconfigured to implement different functions.

Additionally, O'Brien (column 3, line 58-64) states that there is flexibility in choosing various operating parameters. This feature does not describe real time reconfiguration of the available logic circuits to implement different logic functions. Those familiar with the art will

know that the selection of operating parameters means that a different operating parameter value can be used in conjunction with the same circuit. The operating parameter does not change the function of the circuit, just the calculation it performs. For example, in the setting of power levels, the power level circuit still performs a power level function, i.e., the output power level being determined by the operating parameter. This is not the same as in Applicant's real time reconfigurable application where the function of a logic circuit is changed to implement a new and different function.

All the references to "topologies" and flexibility refer to the number of output stages. This refers to the number of analog outputs, which can be power MOSFET, half bridged or full bridges. These circuits are not digital. In fact, O'Brien describes (column 3, line 56 to line 64) that the system versatility results from modular design, which allows designers to implement optimum cost-to-performance ratios. However, to achieve this flexibility, as stated (column 3, line 58), the amplifier is implemented in an ASIC and/or FPGA. Therefore, if an ASIC is used, an FPGA must also be used to provide the flexible design features. If only an FPGA is used, then this is used to provide the flexible modular design, as an FPGA can be programmed at design time to implement a specific configuration of the amplifier. This is

not real time reconfiguration, just an implementation of a specific configuration of an amplifier in which a designer decides at design time how many output stages they would like. The code of this particular configuration is then used to implement that particular configuration in an FPGA. Another designer could use the same modular architecture to implement another amplifier, based on the same modular design, to implement an amplifier with a different number of outputs. However, as stated previously, this level of "configuration" is not real time dynamic reconfiguration of the logic circuits during operation to implement different logic function, as described and claimed in Applicant's application. It is just design time configurable.

As described in O'Brien(column 2, line 12), the invention provides a topology. This is singular and implies that no reconfiguration takes place at all during apparatus operation. As outlined above, a specific topology is decided at production time and not during device operation as described in our real time reconfigurable pre-amplifier.

With regards the use of memory in paragraph 4 of the office action, Applicant's claimed memory is used to store configuration data to control the configuration of Applicant's real time reconfigurable logic. As outlined previously, the ASIC described in O'Brien is used to store data parameters

because the ASIC does not perform any real time reconfiguration of its logic circuits. Therefore, the use of memory by O'Brien is not for real time reconfiguration as described and claimed in the present application. Also, as the ASIC described in O'Brien does not perform real time reconfiguration, the use of a host processor or DSP cannot be used for the purpose of updating any configuration memory as there is no such memory. In Applicant's description, the use of a host processor or DSP to update the configuration memory in real time is specifically mentioned. This use of a DSP or host processor is different to that described by O'Brien.

In fact, O'Brien (column 1, lines 50-55) states that the use of an expensive DSP Processor is not required. The processing algorithm can be (if desired) performed in a DSP or "host processor" as well. These sentences describe the use of a conventional DSP to run a conventional software algorithm. They do not describe the use of a DSP or host processor to perform the updating of configuration memory in real time to reconfigure the logic functions as outlined in Applicant's application. The use of the host processor or DSP as described in O'Brien is very different to that described in Applicant's application and, as stated in O'Brien, is not required.

It is therefore submitted that claim 1, as well as all the claims dependent therefrom, are patentable over O'Brien, at least because of the recitation of a "reconfigurable circuit means which are configured in real time under control of configuration data".

All of the other prior art rejections are traversed for the reason that the rejected claims depend from claim 1, and should be considered allowable along therewith. Moreover, a number of these claims define further novel features of the invention that are not disclosed in the applied references.

For example, claim 8 specifies that the apparatus is configured for simultaneous use by more than one user where signal data from one or more signal sources is processed and output to one or more output circuits.

The rejection of claim 8 was based on the view that it would be obvious that one or more users may listen to the output of a speaker. However, the claimed apparatus allows the processing of signals from one or more sources at essentially the same time, allowing more than one user to access the same piece of equipment. This is another advantage of the real time reconfiguration of the logic circuits. Normally, as cited by O'Brien, two users would require two separate pieces of equipment to process two different signal

sources simultaneously. It is therefore submitted that claim 8 is not suggested by, and hence not obvious, over the applied references.

If the above amendment should not now place the application in condition for allowance, the Examiner is invited to call undersigned counsel to resolve any remaining issues.

Respectfully submitted,

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